CLAIMS

1. A memory cell comprising:

a substrate including silicon;

a storage device formed on the substrate, the storage device having a first current-carrying electrode coupled to the substrate, a second current-carrying electrode coupled to a power source and a control electrode; and

an access element formed on the storage device and having a control electrode coupled to a word line, a first current-carrying electrode coupled to the control electrode of the storage device and a second current-carrying electrode coupled to a bit line.

2. The memory cell of claim 1 wherein the access element comprises a vertical MOS FET.

3. The memory cell of claim 1 wherein the access element comprises:

a p-type layer formed on the substrate;

a region of n-type material formed on the p-type layer;

a p+-type region formed on the n-type region;

a trench extending through the p+-type region and the n-type material and into the p-type layer;

a gate oxide extending along a side of the trench from the p+-type region across the n-type region to the p-type layer; and

a gate formed on the gate oxide.

4. The memory cell of claim 1 wherein the substrate comprises n+-type silicon.

5. The memory cell of claim 1 wherein:

the access element comprises a vertical MOS FET; and

the storage device comprises a bipolar transistor that is formed in a source of the access element.

6. The memory cell of claim 1 wherein:

the access element comprises a vertical PMOS FET;

the substrate comprises n+-type silicon; and

the storage device comprises a bipolar transistor formed in a source of the access element.

7. A memory device having an address bus and a data terminal, comprising:

an array of memory cells formed on a substrate including silicon, the memory cells arranged in rows and columns, each of the rows having a word line and each of the columns having a bit line;

a row address circuit coupled to the address bus for activating the word line in the array corresponding to a row address applied to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling a data bus line for the array to the bit line corresponding to a column address applied to the column address circuit through the address bus; and

a sense amplifier having an input coupled to a bit line and an output coupled to the data terminal of the memory device, wherein each memory cell comprises:

an access element having a control electrode coupled to one of the word lines, a first current-carrying electrode coupled to the node and a second current-carrying electrode coupled to one of the bit lines; and

a storage device formed on the substrate and stacked vertically with the access element, the storage device having a first current-carrying

electrode coupled to the substrate, a second current-carrying electrode coupled to a power source and a control electrode coupled to the access element.

8. The memory device of claim 7 wherein the memory device comprises a static random access memory.

9. The memory device of claim 7 wherein:

the access element comprises a vertical PMOS FET; and

the storage device comprises a NPN bipolar transistor that is formed in a source of the access element.

10. The memory device of claim 9 wherein the vertical PMOS FET and the storage device are formed in an area equal to four squares, where each side of each square is as long as a critical dimension of the device.

11. The memory device of claim 7 wherein the substrate includes a n+-type surface layer and the access element comprises:

a p-type layer formed on the substrate;

a region of n-type material formed on the p-type layer;

a p+-type region formed on the n-type region;

a trench extending through the p+-type region and the n-type region and into the p-type layer;

a gate oxide extending along a side of the trench from the p+-type region across the n-type region to the p-type layer; and

a gate formed on the gate oxide.

12. The memory device of claim 7 wherein the storage device is formed underneath the access element.

13. A memory cell comprising:

a substrate including silicon;

an access element comprising a vertical MOS FET formed on the substrate and having a control electrode coupled to a word line, a first current-carrying electrode and a second current-carrying electrode coupled to a bit line; and

a storage device formed in a source of the access element and having a control electrode coupled to the first current-carrying electrode of the access element.

14. The memory cell of claim 13 wherein the storage device is formed on the substrate and has a first current-carrying electrode coupled to the substrate and a second current-carrying electrode coupled to a power source.

15. The memory cell of claim 13 wherein the access element comprises a vertical MOS FET.

16. The memory cell of claim 13 wherein the access element comprises:

a p-type layer formed on the substrate;

a region of n-type material formed on the p-type layer;

a p+-type region formed on the n-type region;

a trench extending through the p+-type region and the n-type region and into the p-type layer;

a gate oxide extending along a side of the trench from the n+-type region across the n-type region to the p-type layer; and

a gate formed on the gate oxide.

17. The memory cell of claim 13 wherein the substrate comprises n+-type silicon.

18. The memory cell of claim 13 wherein the storage device is formed beneath the access element.

19. A memory comprising:

addressing means having a first set of terminals coupled to a first external port and a second set of terminals coupled to a memory array, the addressing means for targeting one or more memory cells within the memory array; and

data conditioning means coupled to a second external port and to the memory array, the data conditioning means for reading data from or writing data to the one or more targeted memory cells, wherein each memory cell comprises:

a storage device formed on the substrate and including a first current-carrying electrode coupled to the substrate, a second current-carrying electrode coupled to a power source and a control electrode; and

access means formed on the storage device and having a control electrode coupled to a word line, a first current-carrying electrode coupled to the control electrode of the storage device and a second current-carrying electrode coupled to a bit line.

20. The memory of claim 19 wherein the memory comprises a SRAM.

21. The memory of claim 19 wherein the access device comprises a PMOS FET and the storage device comprises a NPN bipolar transistor formed in a source of the access device.

22. The memory of claim 20 wherein the first current-carrying electrode of the storage device is an emitter and the second current-carrying electrode of the storage device is a collector.

23. The memory of claim 19 wherein the access means comprises a vertical MOS FET.

24. The memory of claim 19 wherein the access means and the storage means are formed in an area equal to four squares, where each side of each square is as long as a critical dimension.

25. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus and adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

at least one array of memory cells arranged in rows and columns, each of the rows having a word line and each of the columns having a bit line;

a row address circuit adapted to receive and decode a row address, and select a row of memory cells corresponding to the row address;

a column address circuit adapted to couple the bit line for the column corresponding to a column address to data bus to receive or apply data to one of the memory cells in the selected row corresponding to a column address; and

a data path circuit adapted to couple data between an external data terminal and each of the bit lines for respective columns, the data path circuit including a sense amplifier having an output coupled to the external data terminal of the memory device and an input, wherein each of the memory cells comprises a storage device formed from silicon and coupled between first and second reference voltages and an access device formed on the storage device and having a first current-carrying electrode coupled to a control electrode of

the storage device, a control electrode coupled to one of the word lines and a second current-carrying electrode coupled to one of the bit lines.

26. The computer system of claim 25 wherein the memory device comprises a static random access memory.

27. The computer system of claim 25 wherein the access device comprises a vertical MOS FET.

28. The computer system of claim 25 wherein the access device and the storage device are formed in an area equal to four squares, where each side of each square is as long as a critical dimension.

29. A method of forming a memory cell comprising:

forming a series of epitaxial layers on a substrate;

etching trenches through the series of epitaxial layers to form a series of bars;

forming an oxide under the bars to electrically isolate the bars from the substrate;

forming a storage device on top of the oxide; and

forming an access element on top of the storage device.

30. The method of claim 29 wherein the act of forming a storage device comprises forming a NPN bipolar transistor.

31. The method of claim 29 wherein the act of forming an access element comprises forming a vertical PMOS FET.

32. The method of claim 29 wherein the act of forming a storage device comprises forming a NPN bipolar transistor in a source of a PMOS FET comprising the access element.